ACM SIGMOD
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Sherman: A Write-Optimized Distributed B+Tree Index on Disaggregated Memory

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Tsinghua University

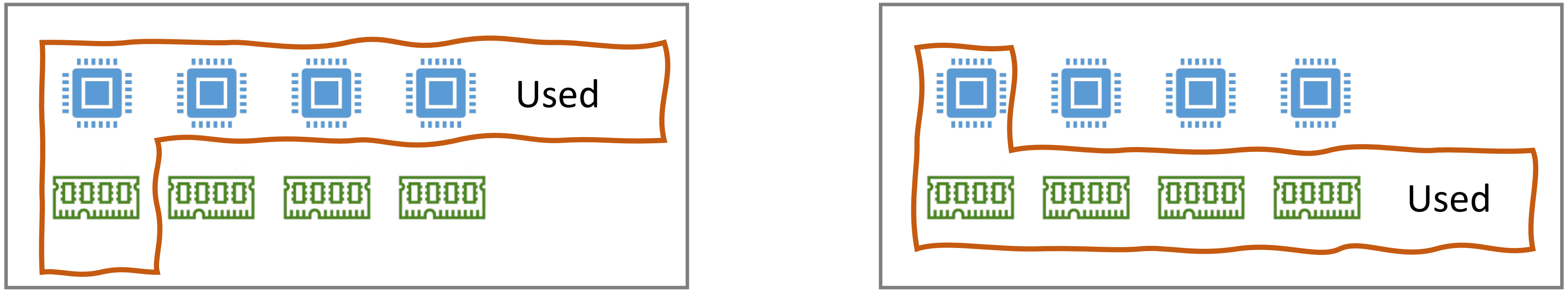
Memory Disaggregation (1)

Problem: low memory utilization in datacenters

- < 65% in Google, Alibaba, and Snowflake[1,2,3]

Root Cause: imbalanced memory usages across servers

- Some servers are CPU-bound, but some are memory-bound
- Cannot use memory beyond a local server



Server 1 (CPU-bound) Server 2 (memory-bound)

[1] Who Limits the Resource Efficiency of My Datacenter: An Analysis of Alibaba Datacenter Traces (IWQoS'19)
[2] Borg: the Next Generation (EuroSys'20)
[3] Memtrade: A Disaggregated-Memory Marketplace for Public Clouds (arXiv'21)

Memory Disaggregation (2)

Memory Disaggregation

- ❖ Physically separate CPU and memory into network-attached components

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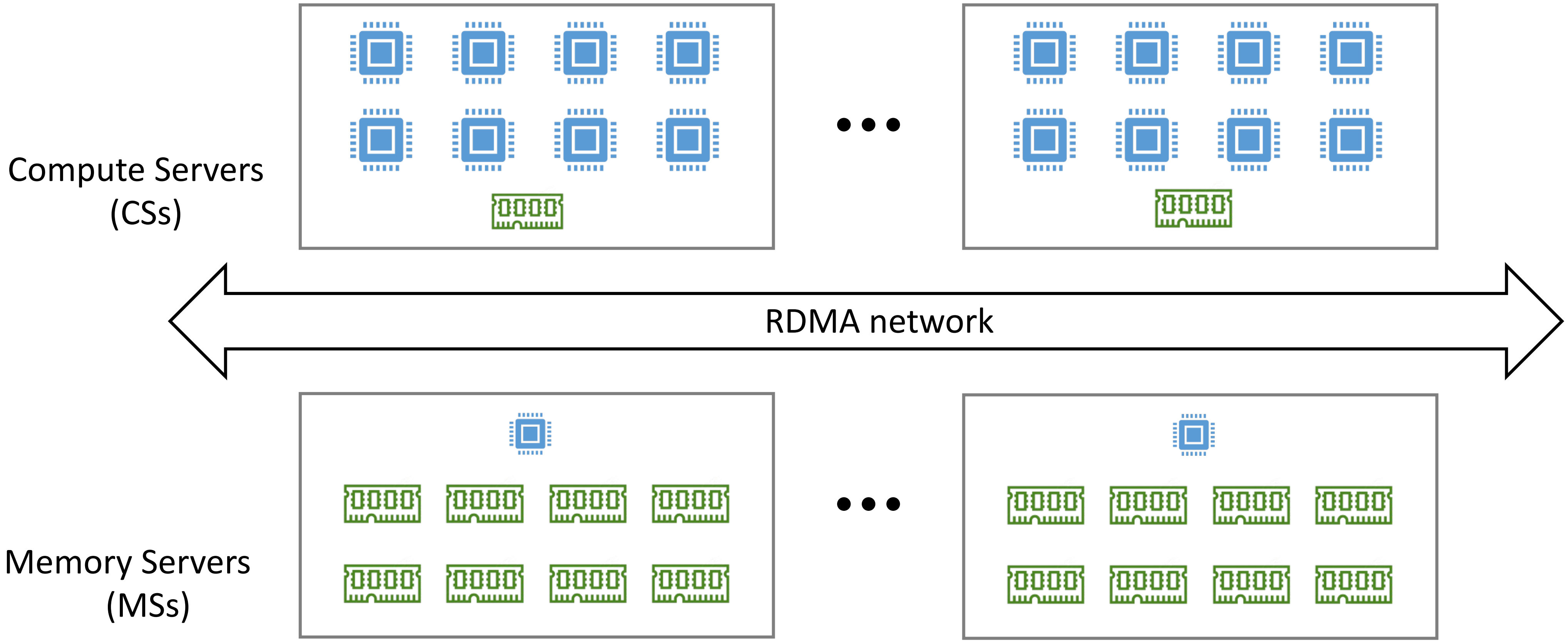

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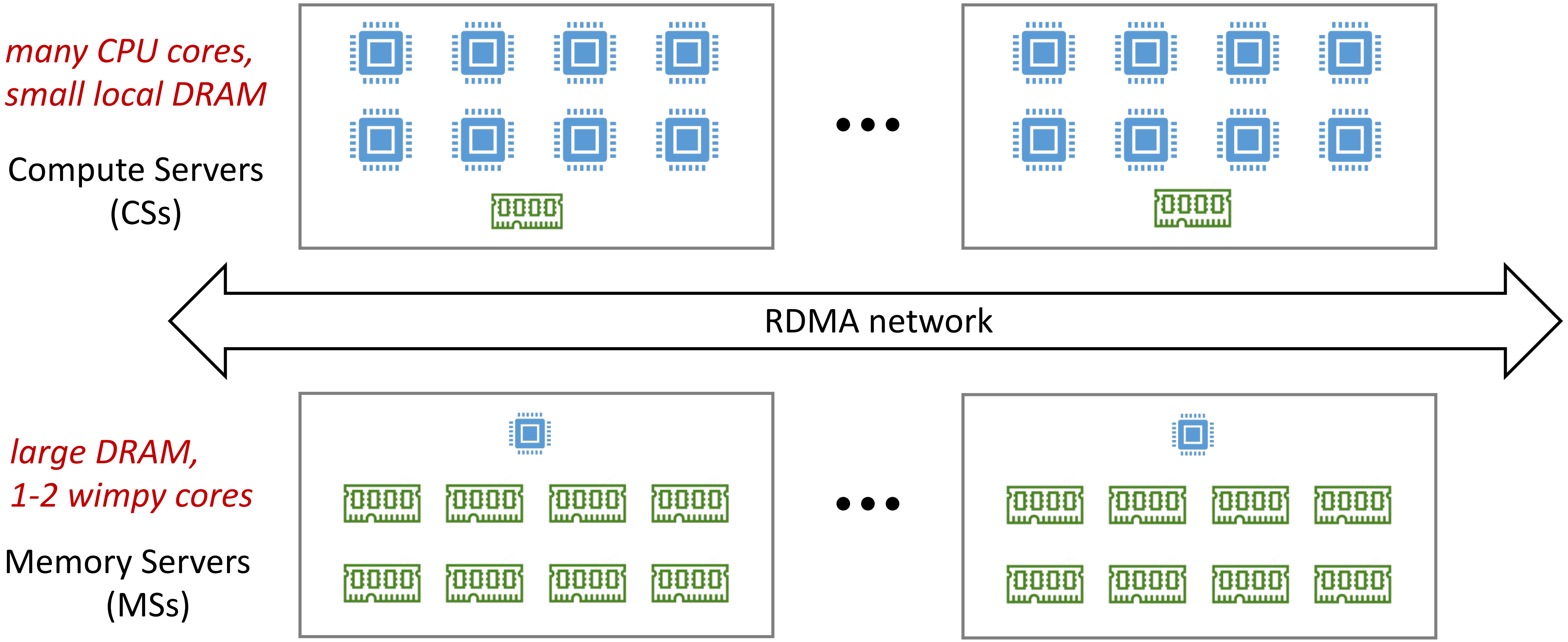

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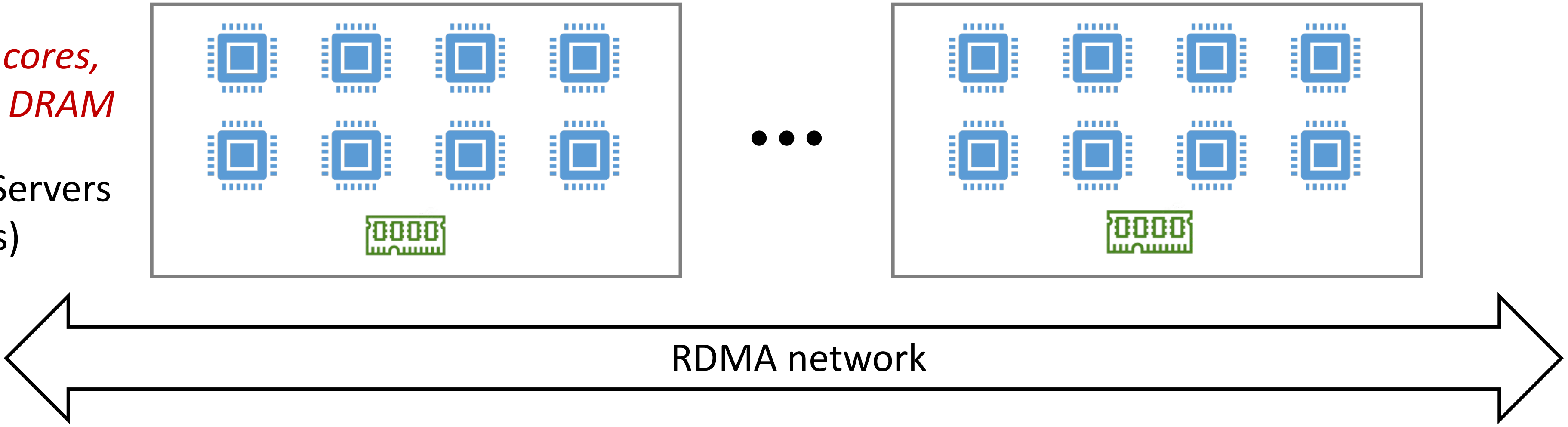
- ❖ Physically separate CPU and memory into network-attached components

many CPU cores,
small local DRAM

Compute Servers
(CSs)



larg
1-2

Mem

Benefits:

- ✓ Independently scaling memory and CPU
- ✓ Flexibly assembling resources for apps
- ✓ Efficiently sharing memory between apps

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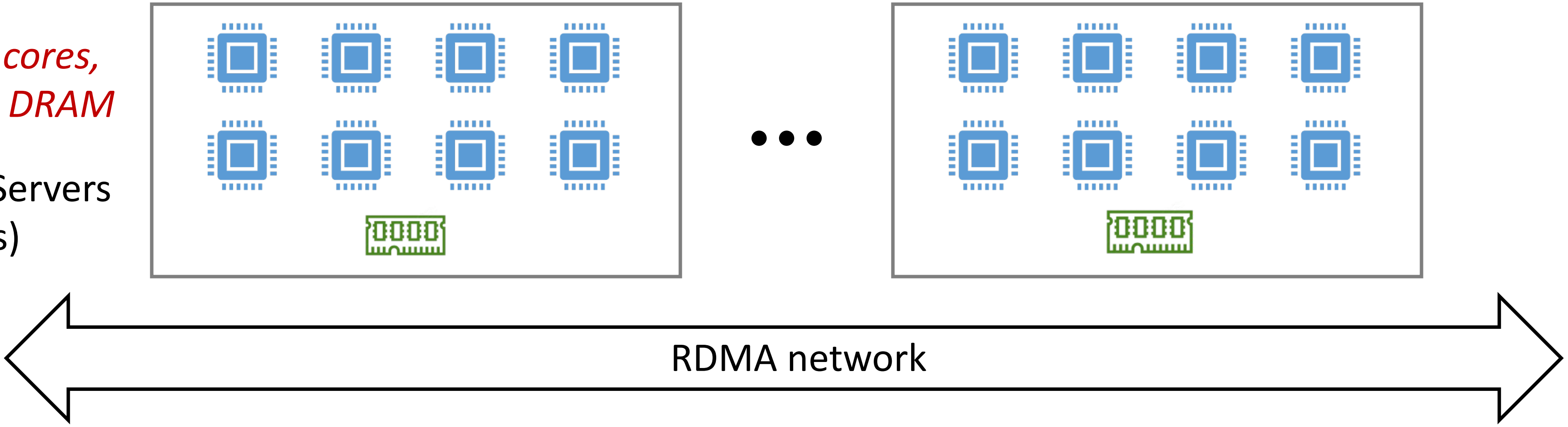

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Mem

Benefits:

✓ Independently scaling memory and CPU
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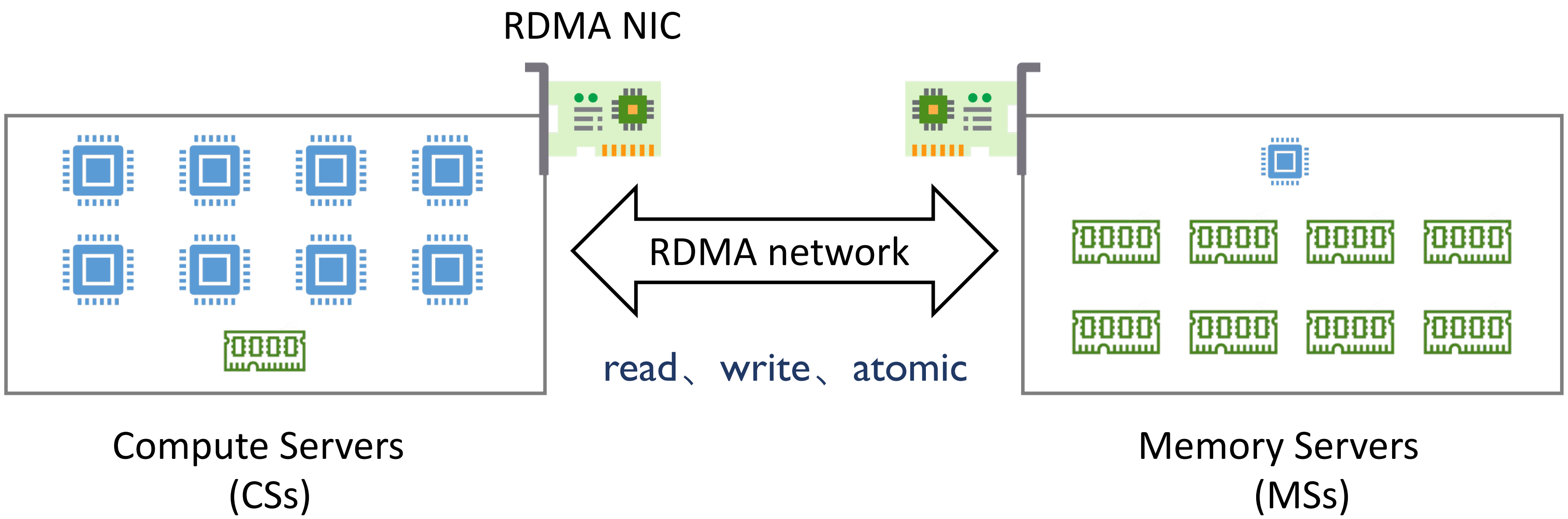
✓ Efficiently sharing memory between apps

→ **high memory utilization**

Memory Disaggregation (3)

Key Enabler: Remote Direct Memory Access (RDMA)

- ❖ High bandwidth: 100/200/400Gbps
- ❖ Low latency: RTT < 2us
- ❖ Directly access remote memory: read、write、atomic (e.g., cas)



Tree Indexes on Disaggregated Memory (1)

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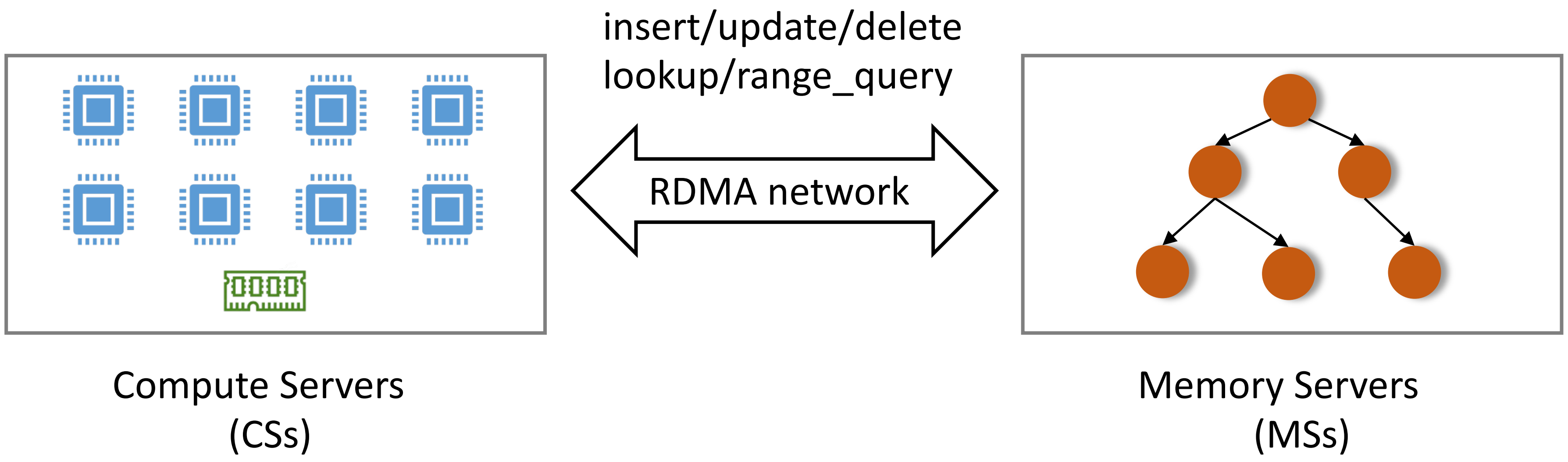

Tree Indexes on Disaggregated Memory (2)

Reexamine Existing RDMA-based Tree Indexes

1. Using RPC to handle index write operations (i.e., insert/update/delete)

   EXAMPLE Cell [ATC'16], FaRM-Tree [SIGMOD'19]

   Issue: Cannot be deployed on DM — near-zero computation power at memory-side

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2. One-sided approach: leveraging RDMA read/write/atomic for all index ops

   EXAMPLE FG [SIGMOD'19]

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FG (Zipf 0.99)	Throughput (Mops)	50th Lat. (us)	99th Lat. (us)
5% Write	31.8	4.9	14.9
50% Write	0.34	10	19890

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3. Hardware modification or SmartNICs for offloading index ops

   EXAMPLE HT-Tree [HotOS'19]

   Issue: High TCO (total cost of ownership)

Our Goal

Our Goal: building a tree index on disaggregated memory
that can deliver high performance (for both read/write ops)
with commodity RDMA NICs

Why One-sided Approach is Slow ? (1)

(1) Excessive Round Trips

cas = compare and swap ; faa = fetch and add

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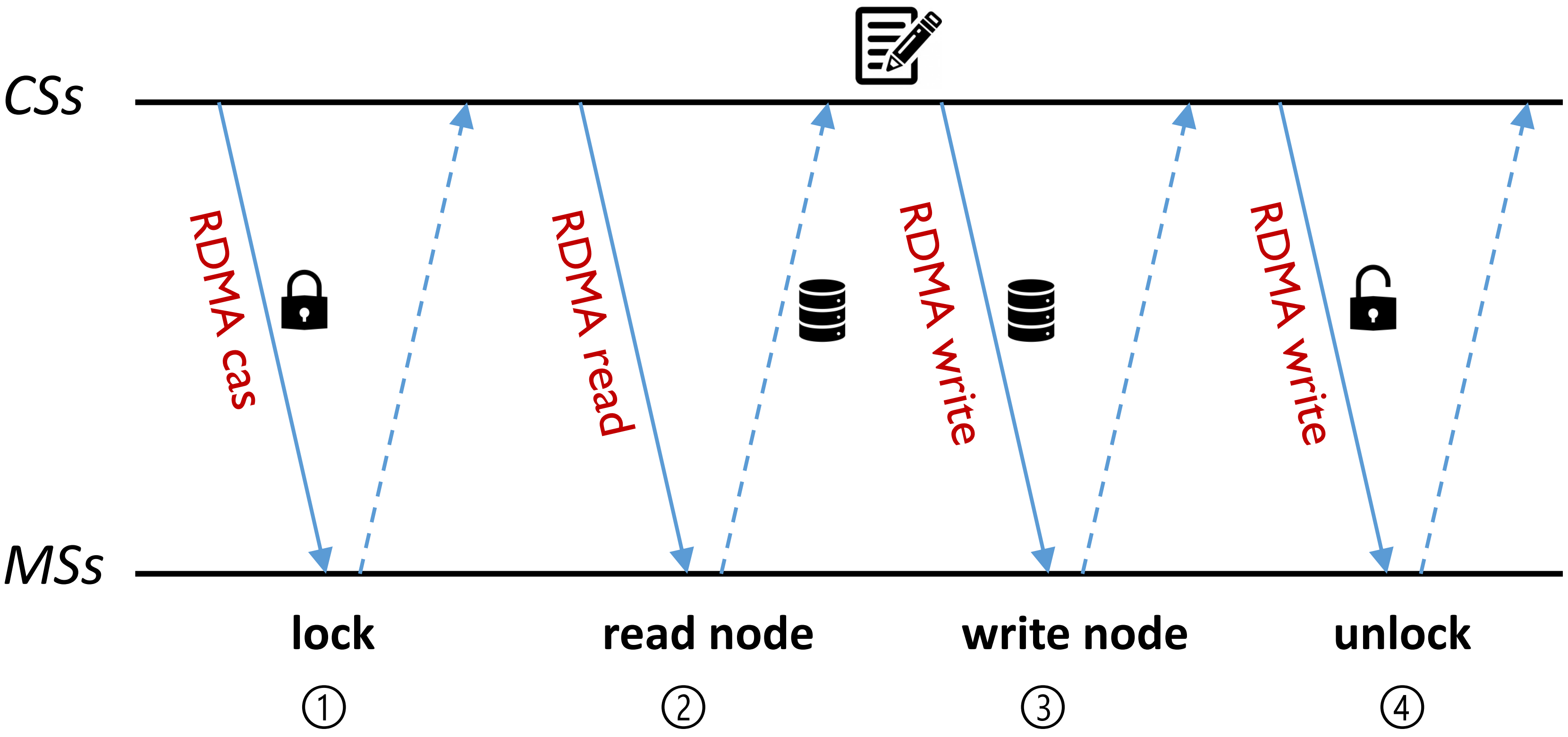
Four round trips when modifying a tree node (FG [SIGMOD'19])



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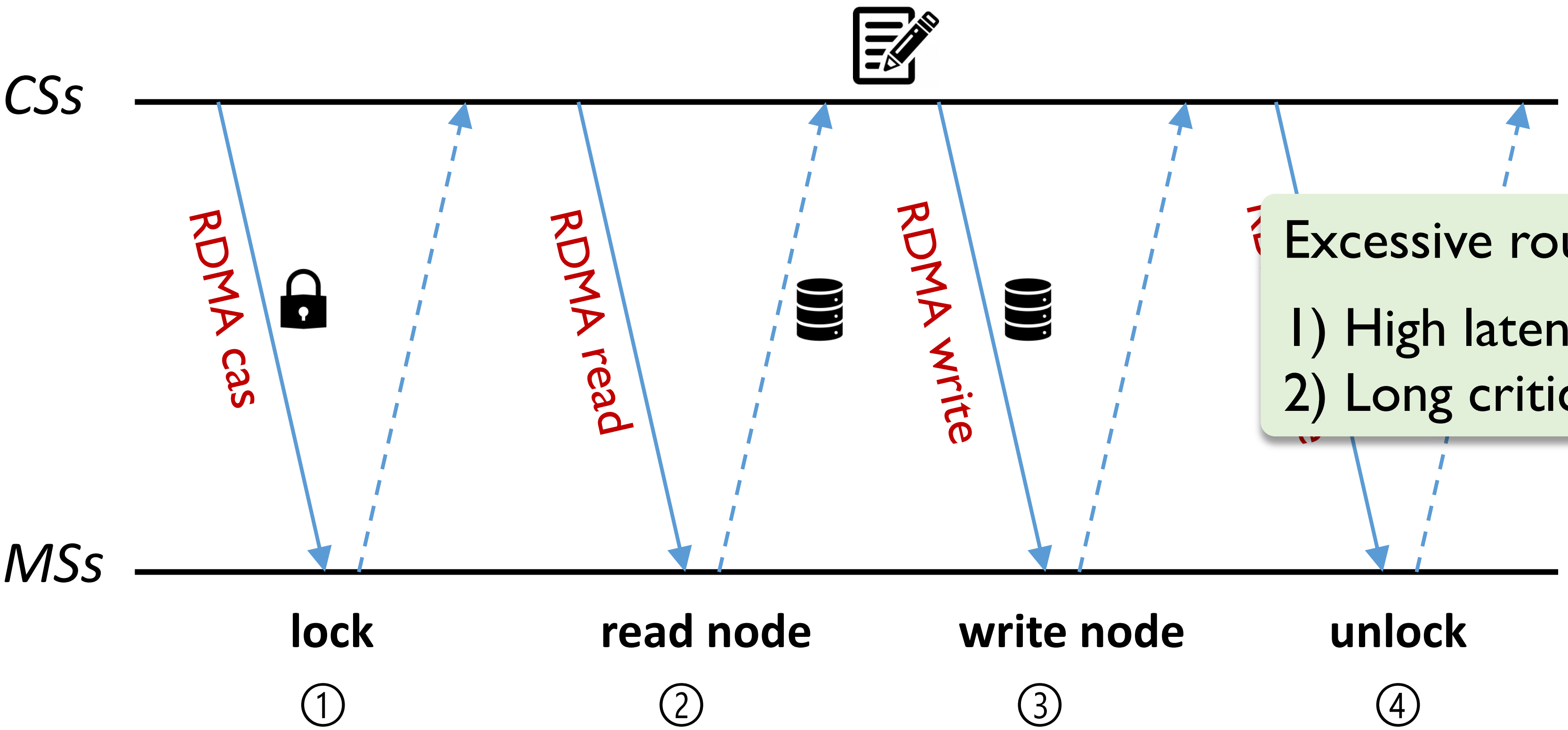

Excessive round trips harm performance:

1) High latency of single write op
2) Long critical path, blocking conflicting ops

cas = compare and swap ; faa = fetch and add

Why One-sided Approach is Slow ? (2)

(2) Slow Synchronization Primitives — RDMA lock

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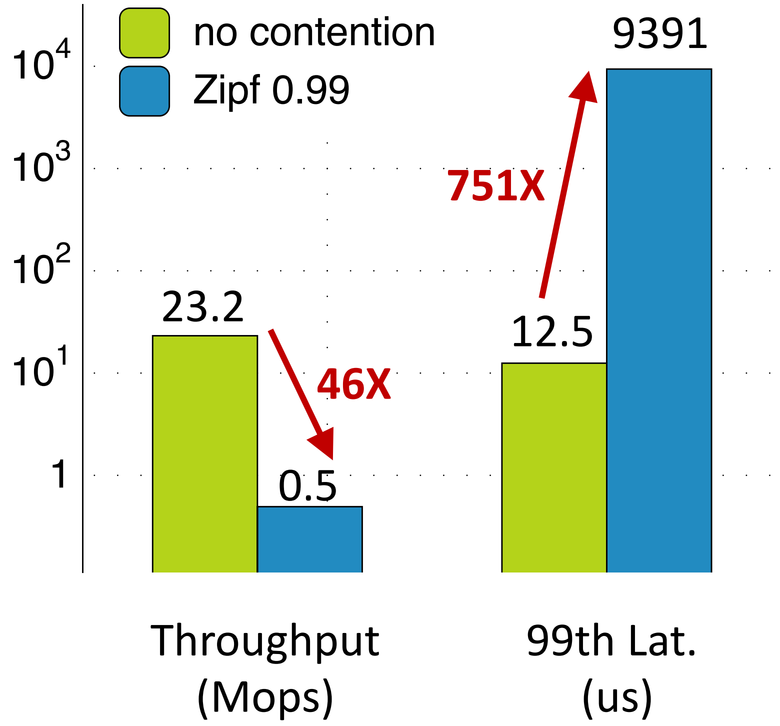

154 threads acquire/release 10240 locks in an MS,
RDMA cas for lock acquisition and faa for release (FG)

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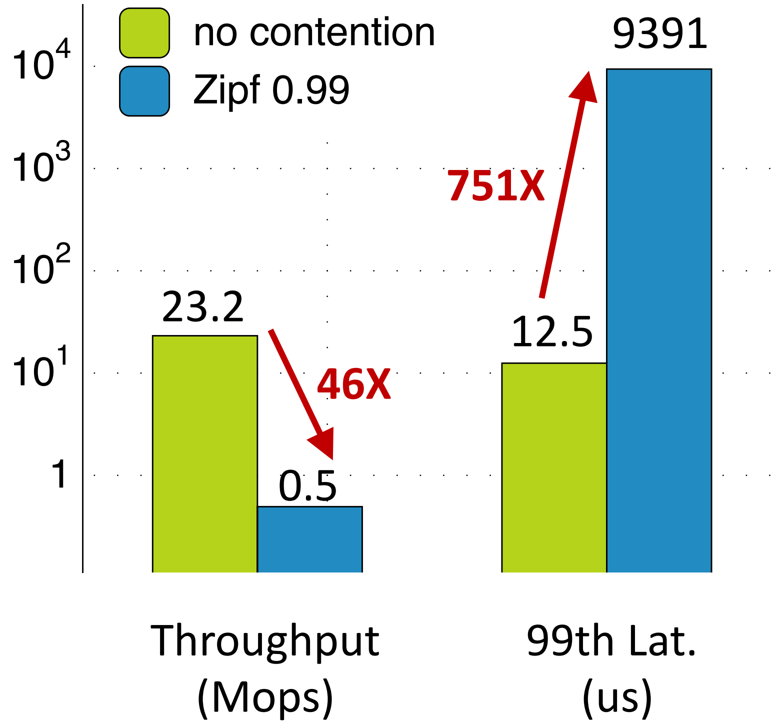

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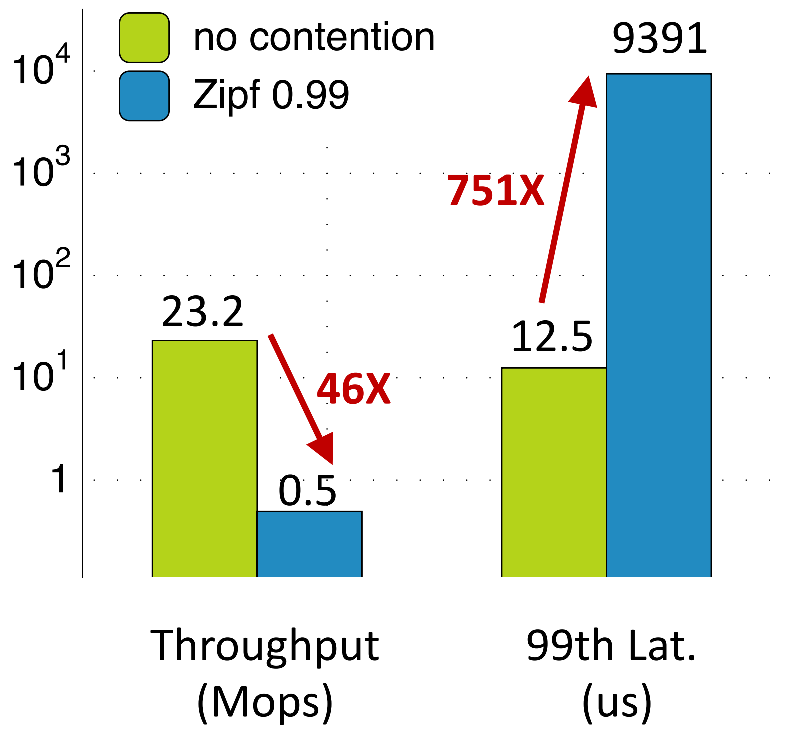

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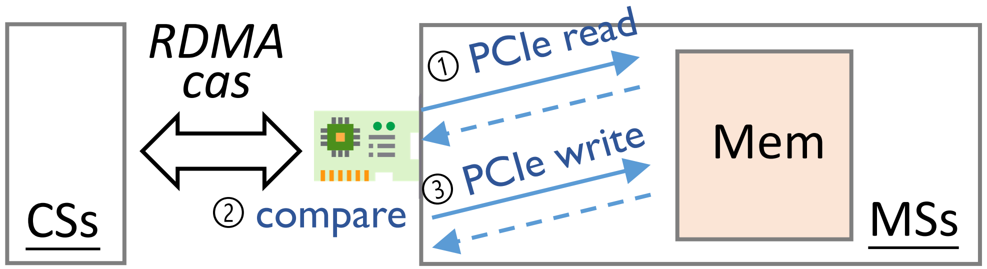
1. Expensive in-NIC concurrency control

- NICs serialize atomic verbs w/ 2-PCIe-txn critical path



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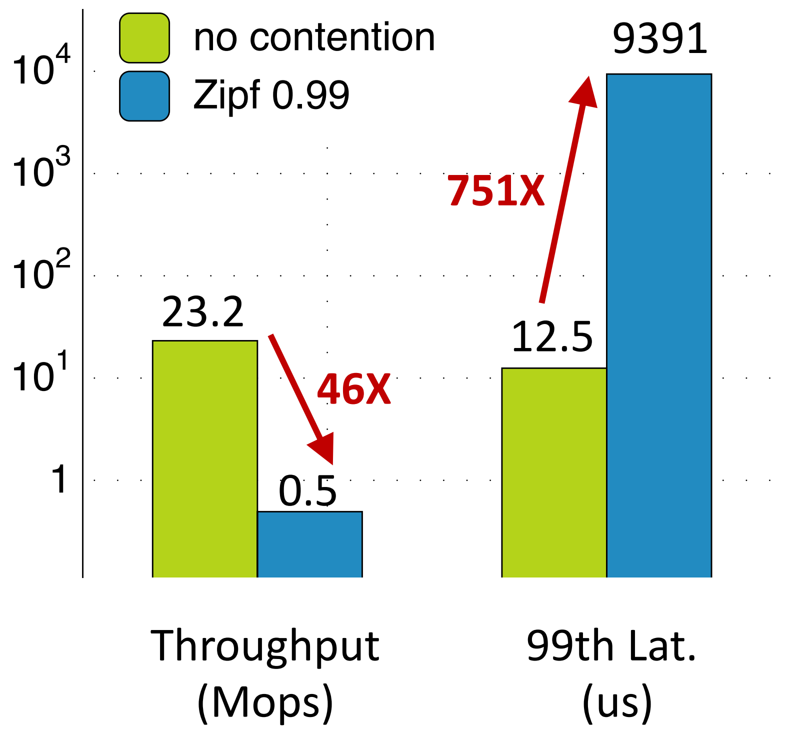

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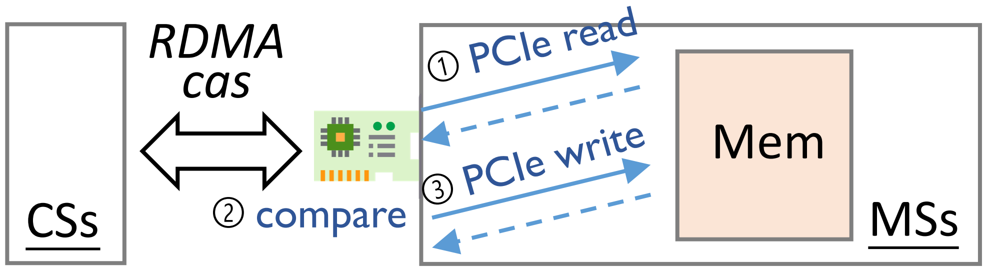

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- Lock retries consume limited RDMA throughput

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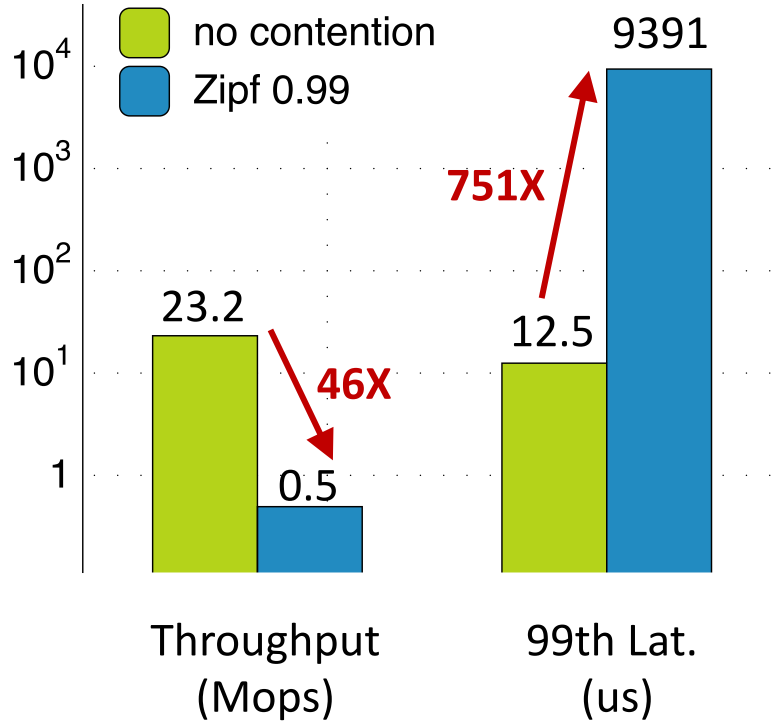

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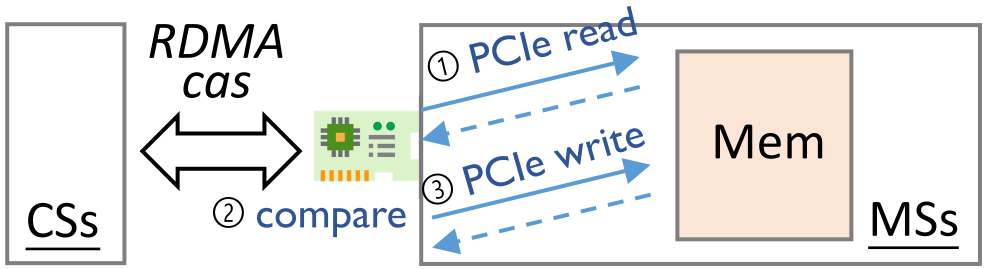

2. Unnecessary retries
- Lock retries consume limited RDMA throughput

3. Lacking Fairness
- Do not consider fairness, starving some clients and further inducing high tail latency

Why One-sided Approach is Slow ? (3)

(3) Write Amplification

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Lots of indexes use lock-free lookup to eliminate read locks:

- Issue RDMA read to fetch tree node
- Detect inconsistent data due to concurrent writes via checksum or versions
- Retry if data is inconsistent

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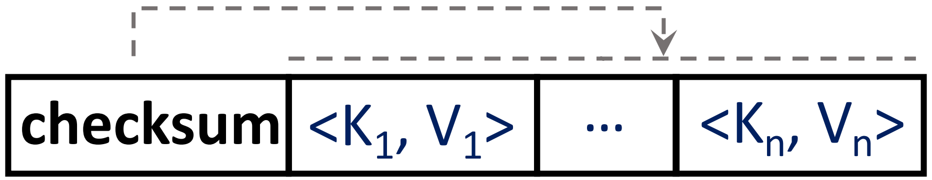

Checksum-based

Writer: modify entries, checksum = *crc*(node)
Reader: if checksum == *crc*(node) ?

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checksum	$<K_1, V_1>$	…	$<K_n, V_n>$

Checksum-based

ver_a	$<K_1, V_1>$	…	$<K_n, V_n>$	**ver_b**

Version-based

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Reader: if checksum == *crc*(node) ?

Writer: ver_a++, modify entries, ver_b++
Reader: if ver_a == ver_b ?

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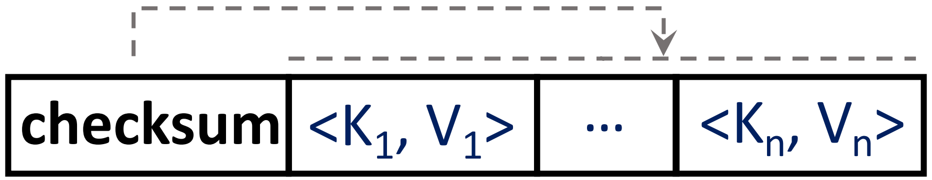


Checksum-based

Version-based

In these two mechanisms, writers must write back the whole tree node, even when modifying an individual KV entry, inducing write amplification

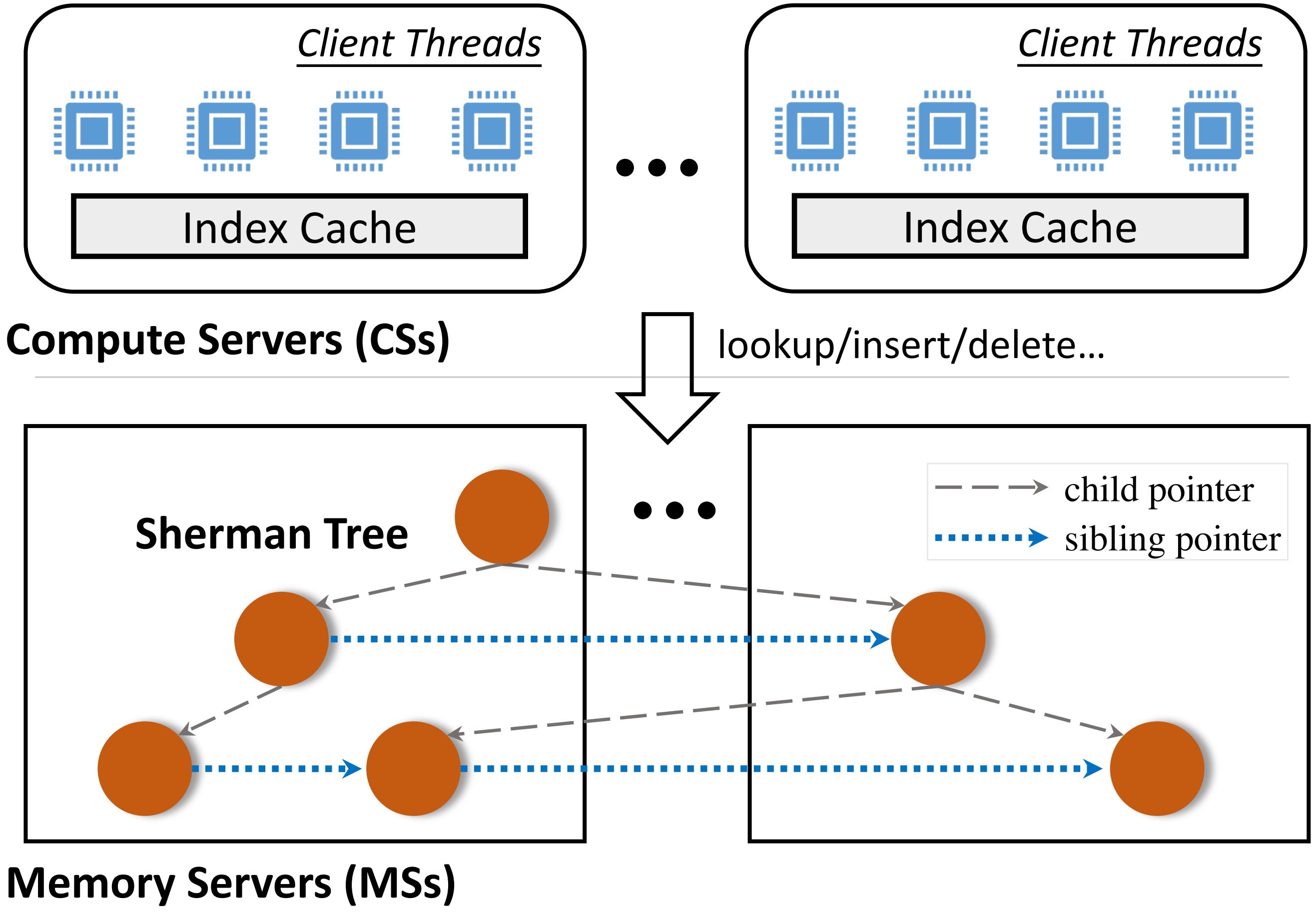
Outline

- Background & Motivation
- Sherman – A Write-Optimized B+Tree on Disaggregated Memory
- Evaluation
- Summary

Sherman Overview

Sherman is a B+Tree index on disaggregated memory

- B-link tree structure (sibling pointer)
- Tree nodes are across many MSs
- One-sided RDMA for *all* index ops
- Index cache at CSs
  - caching internal tree nodes
  - reducing remote accesses
- Concurrency control
  - write-write conflicts:
    - node-grained exclusive locks
  - read-write conflicts:
    - lock-free search w/ versions



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Reducing round trips	→	Command combination
Accelerating concurrent accesses	→	Hierarchical on-chip lock
Mitigating write amplification	→	Two-level version layout

Command combination

Observation: RDMA write commands are executed in order at receivers

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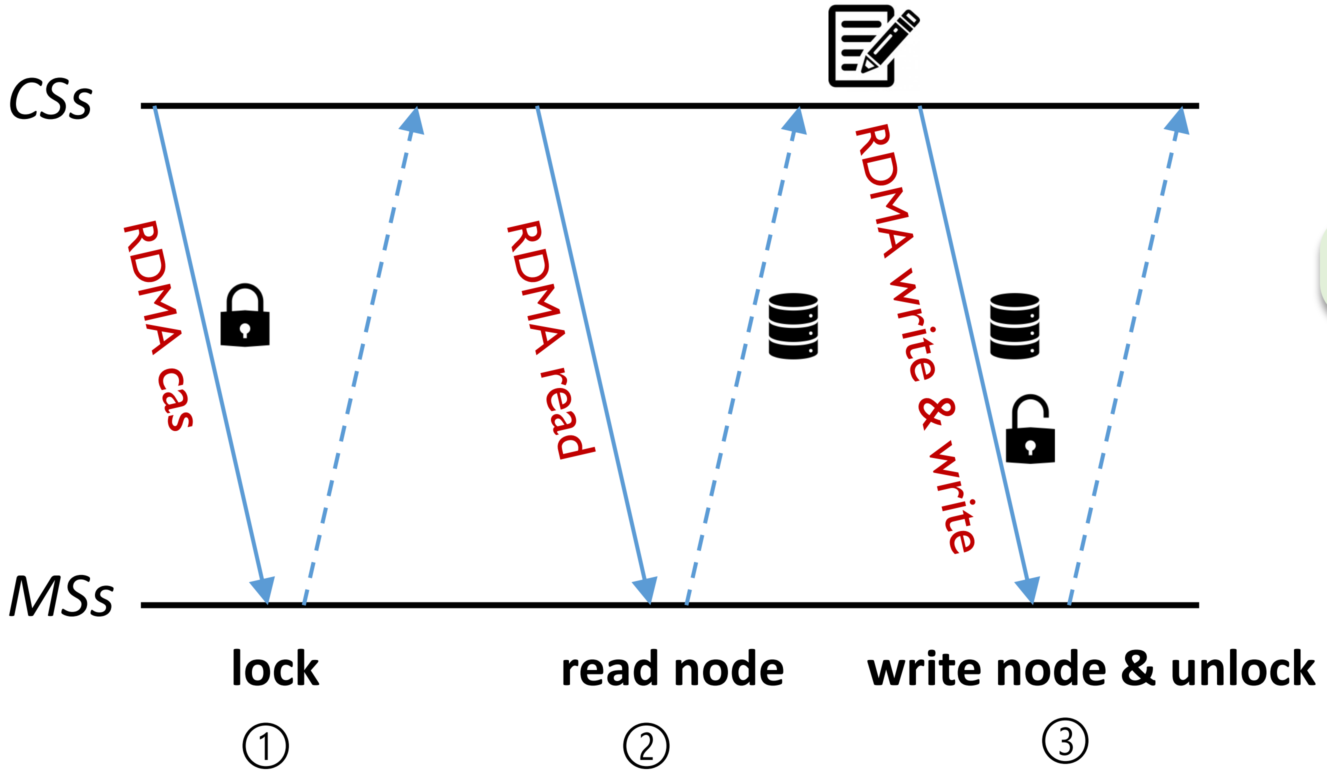

Combine write-back and lock release

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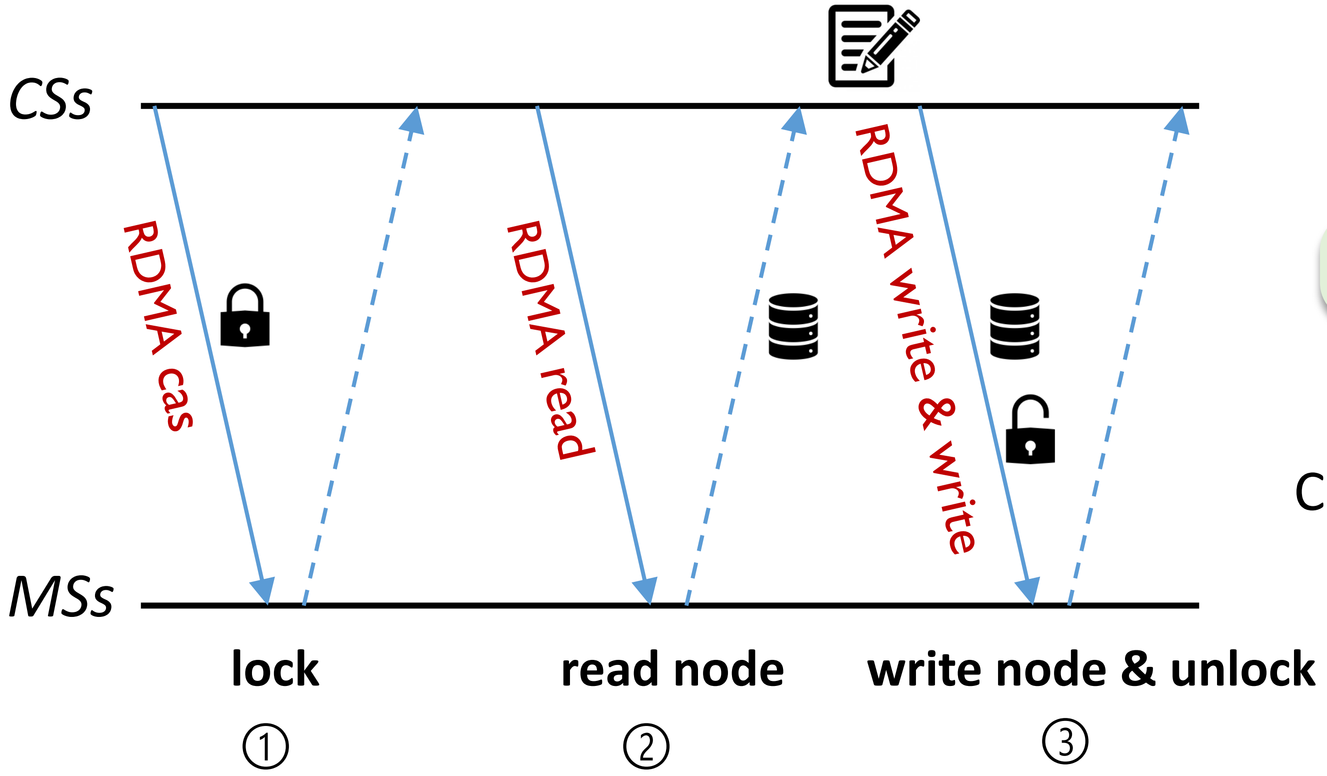

Combine write-back and lock release

Checkout paper for other cases of combination

Hierarchical On-Chip Lock

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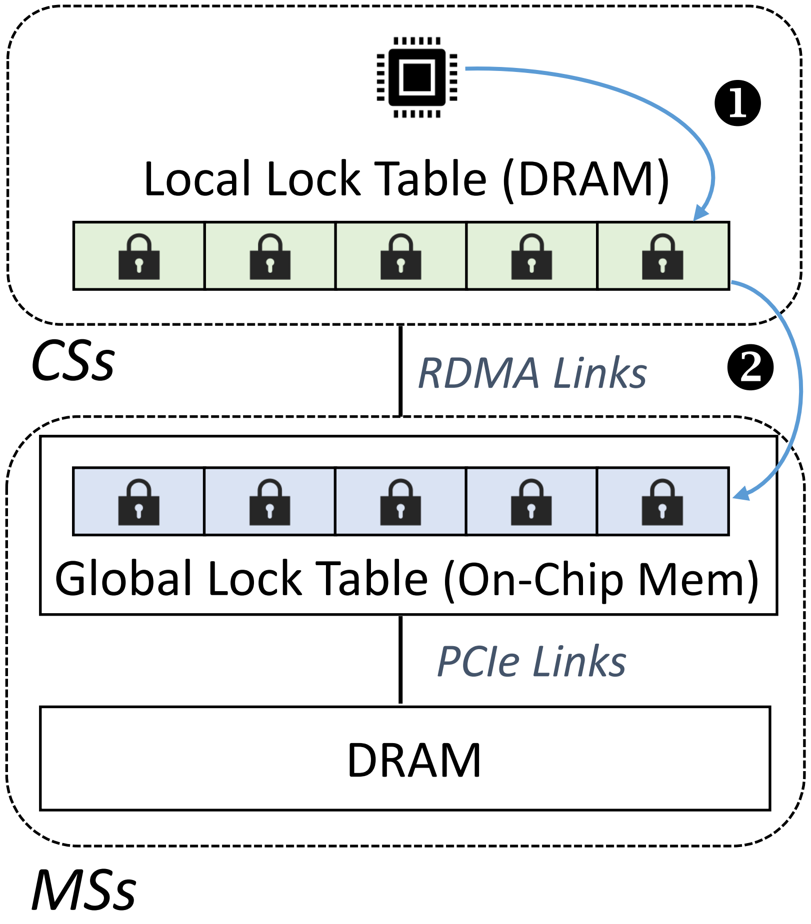

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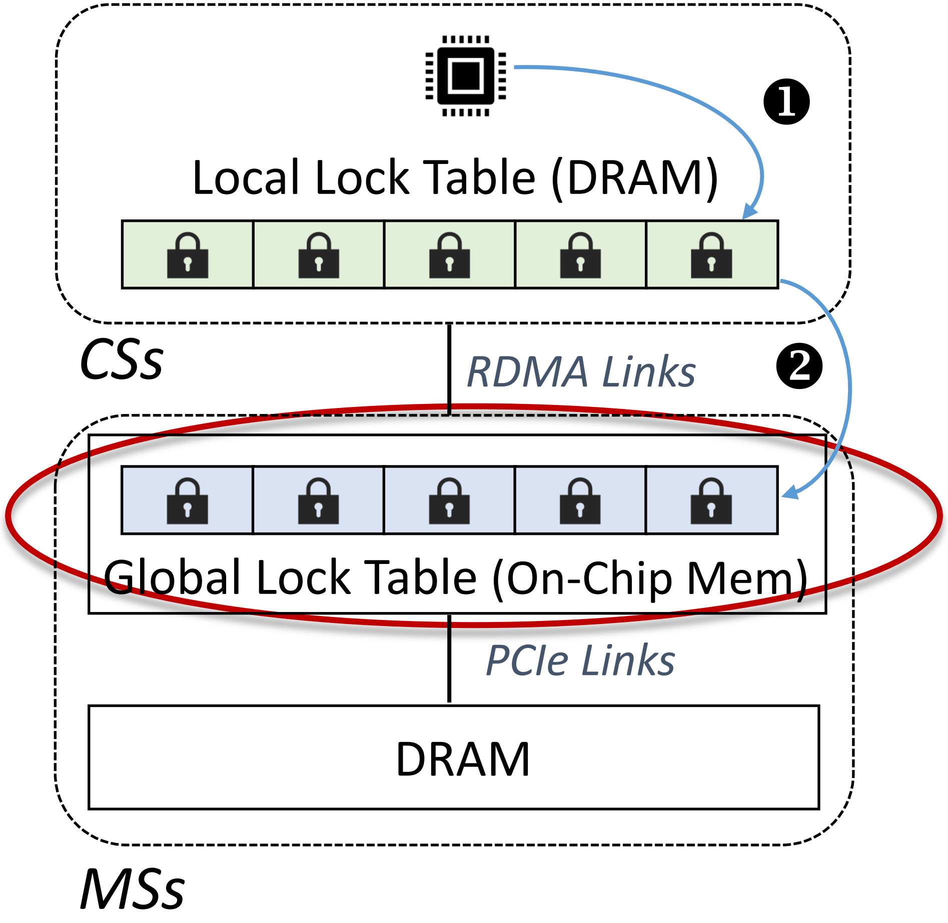
Observation: RDMA NICs can expose on-chip memory (SRAM) for usages

❖ Store locks in on-chip mem of MSs' NICs
- an array called Global Lock Table (GLT)
- hash [addr of tree node] => position in GLT
- eliminate PCIe txn at MSs



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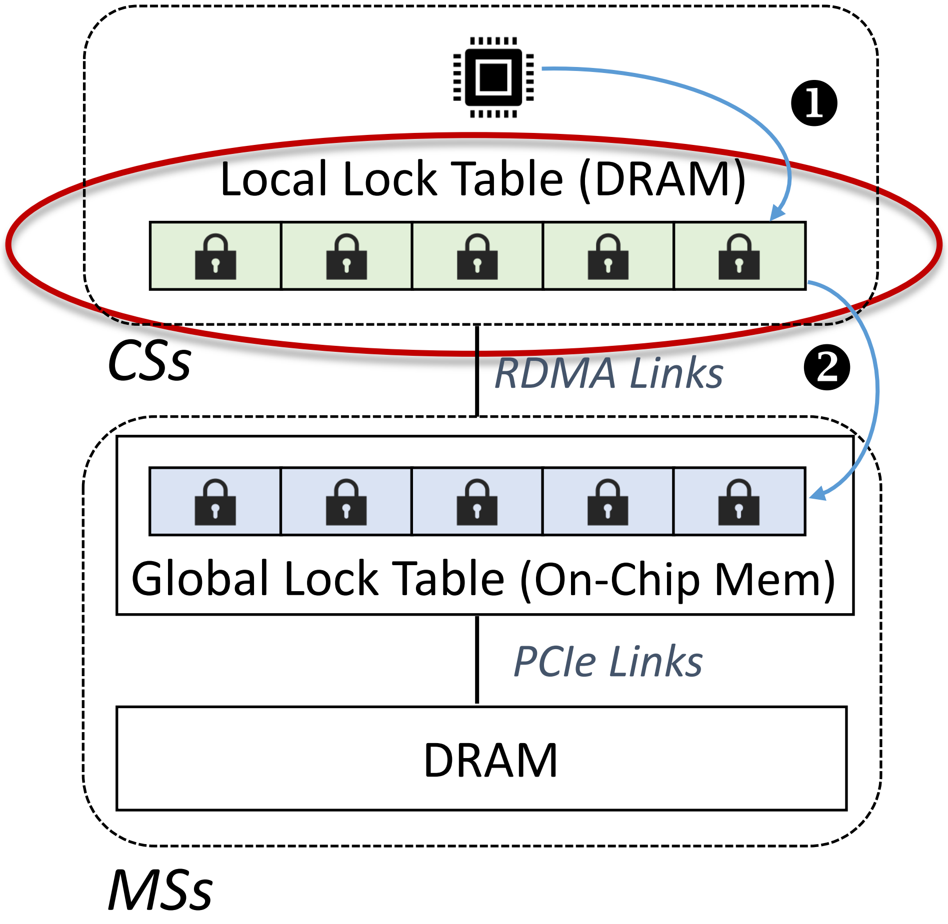

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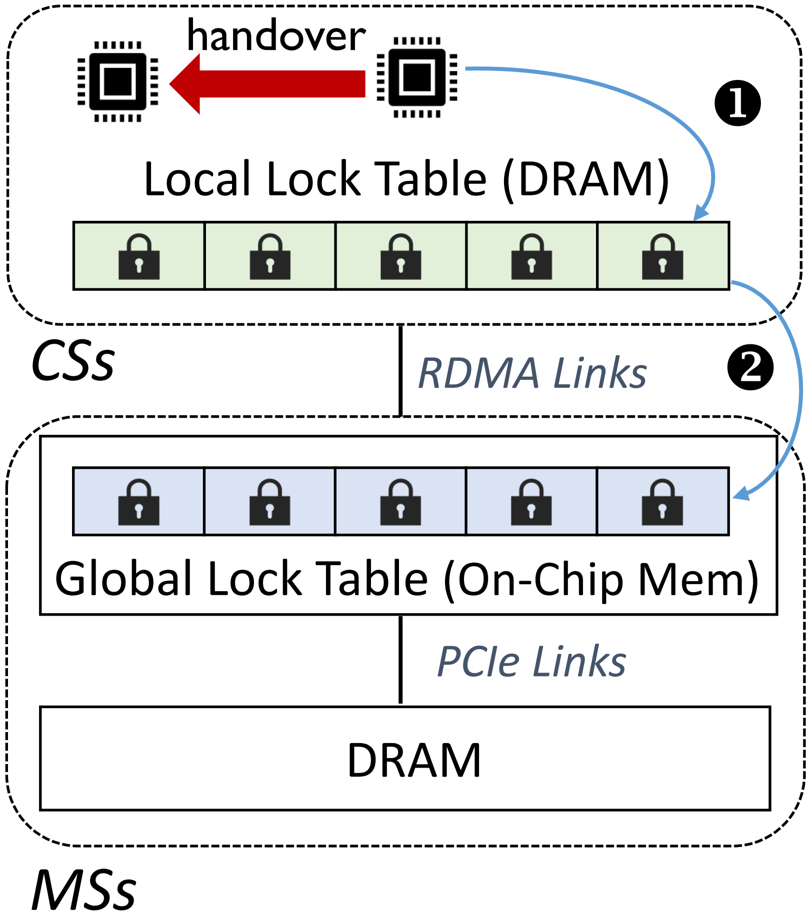
- ❖ Handover mechanism
  - Hand over a lock from one thread to another locally
  - reduce one round trip



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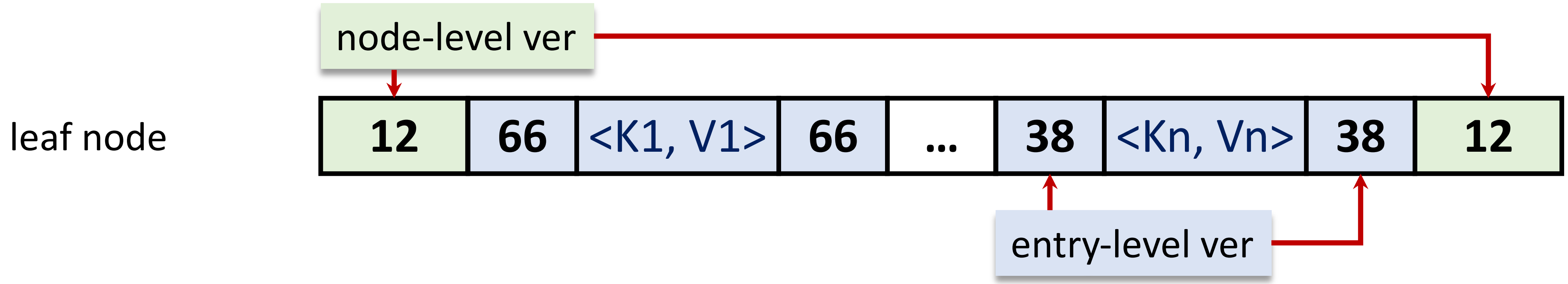

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leaf node

12	**66**	<K1, V1>	**66**	**…**	**38**	<Kn, Vn>	**38**	**12**

write back entry (not node) via RDMA write

update a KV:

67	<K1, V1’>	**67**

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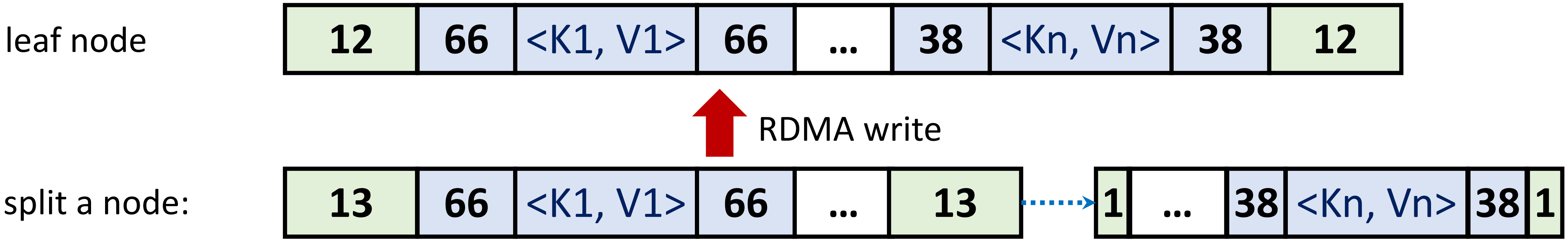

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RDMA read

read a node:	**12**	**66**	<K1, V1>	**66**	**...**	**38**	<Kn, Vn>	**38**	**12**

Whether two node-level vers are equal ? two entry-level vers are equal ? If no, retry

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Experimental Setup

Hardware Platform

Machine * 8

CPU	2 Intel Xeon E5-2650 (12 core)
Mem	128GB DRAM
NIC	100Gbps Mellanox ConnectX-5 w/ 256KB on-chip memory
OS	CentOS 7.7 , Linux kernel 3.10.0

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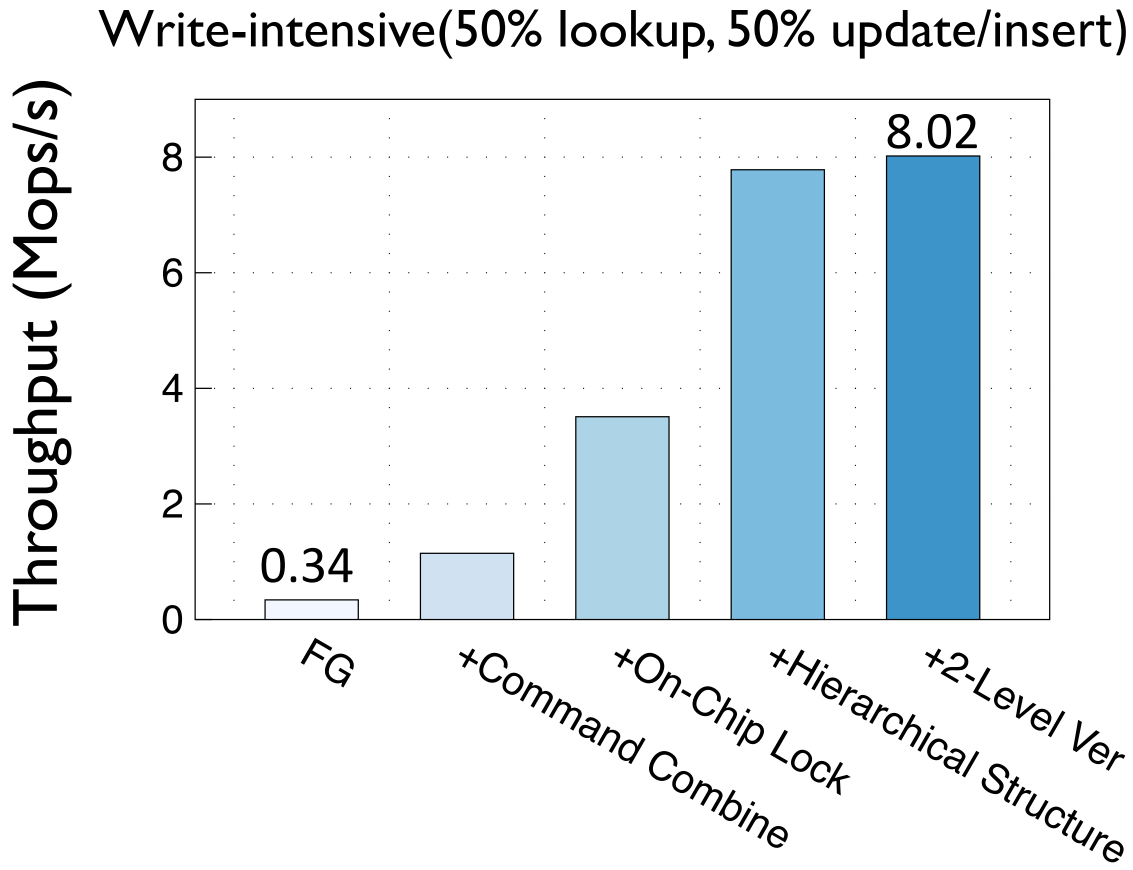
Benchmark: YCSB, Zipfian 0.99; 8B key & 8B value, 1 billion KV; 1KB node; 500MB index cache

Throughput (176 client threads)



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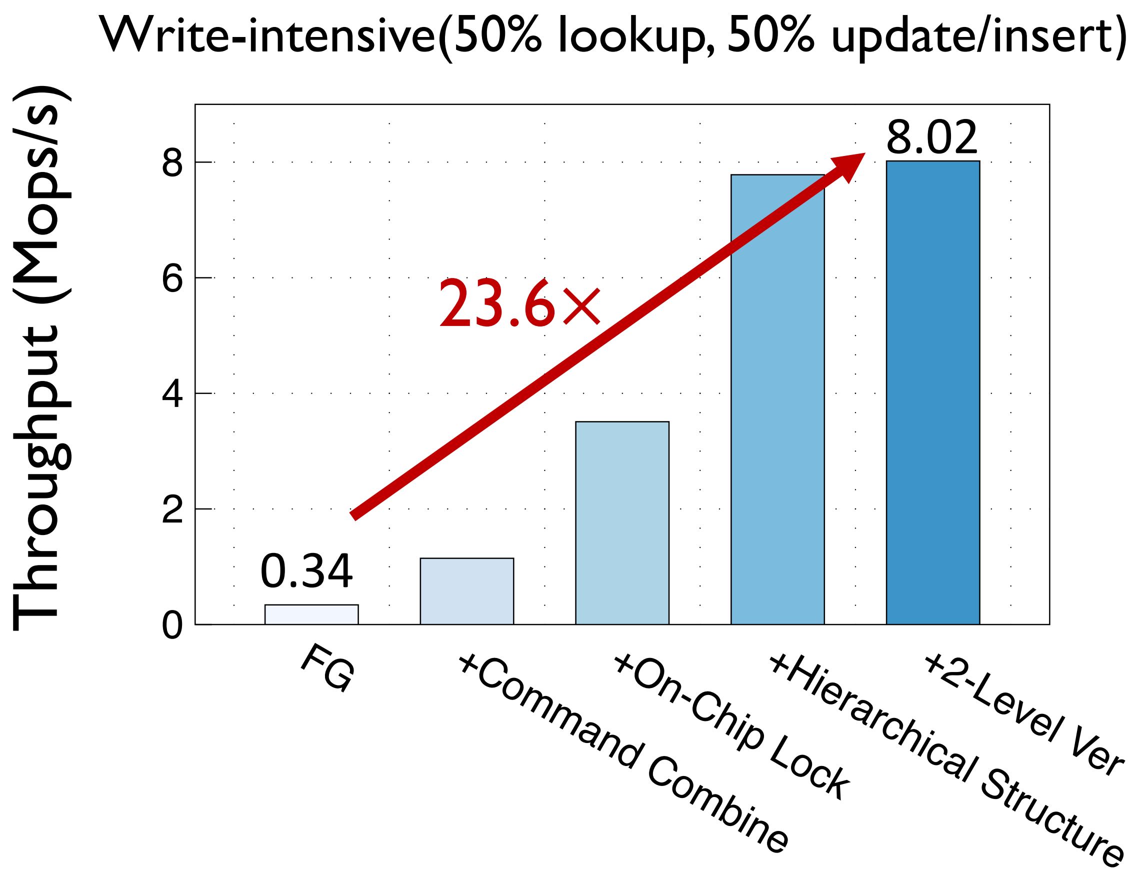

1. Sherman improves throughput significantly under write-intensive workloads
2. All techniques contribute to the high write efficiency

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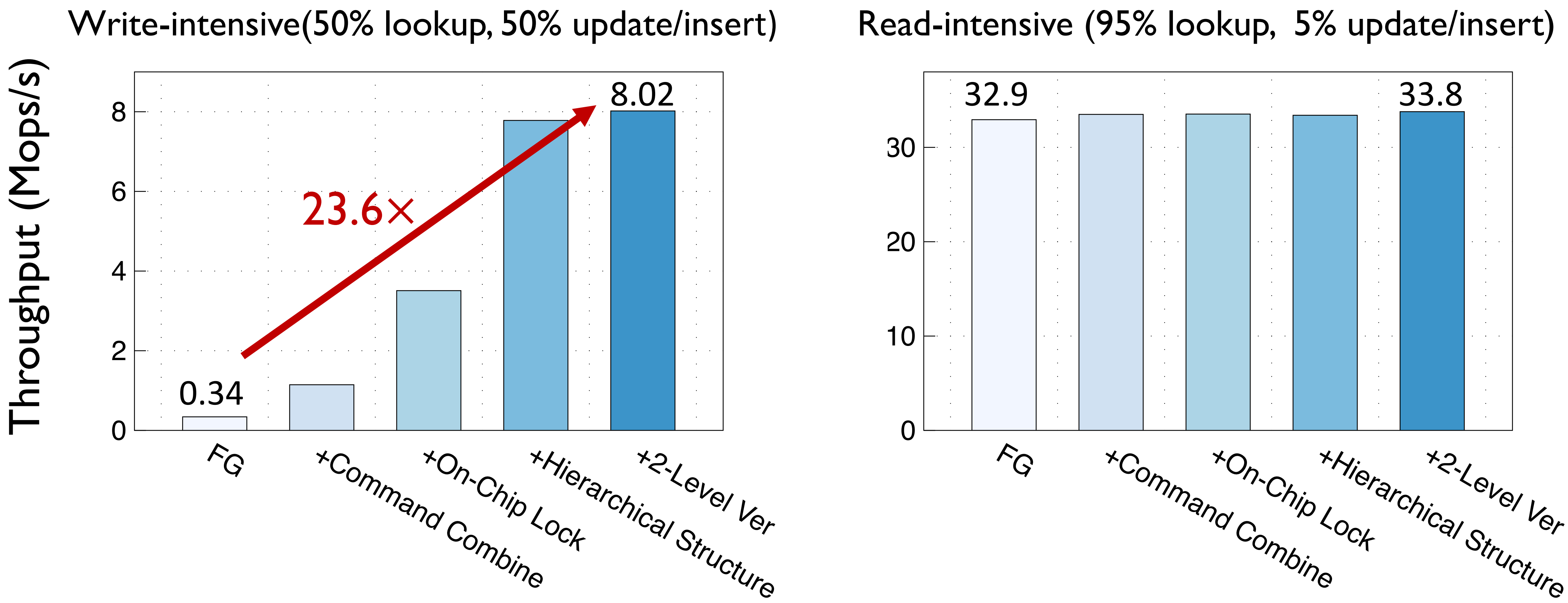

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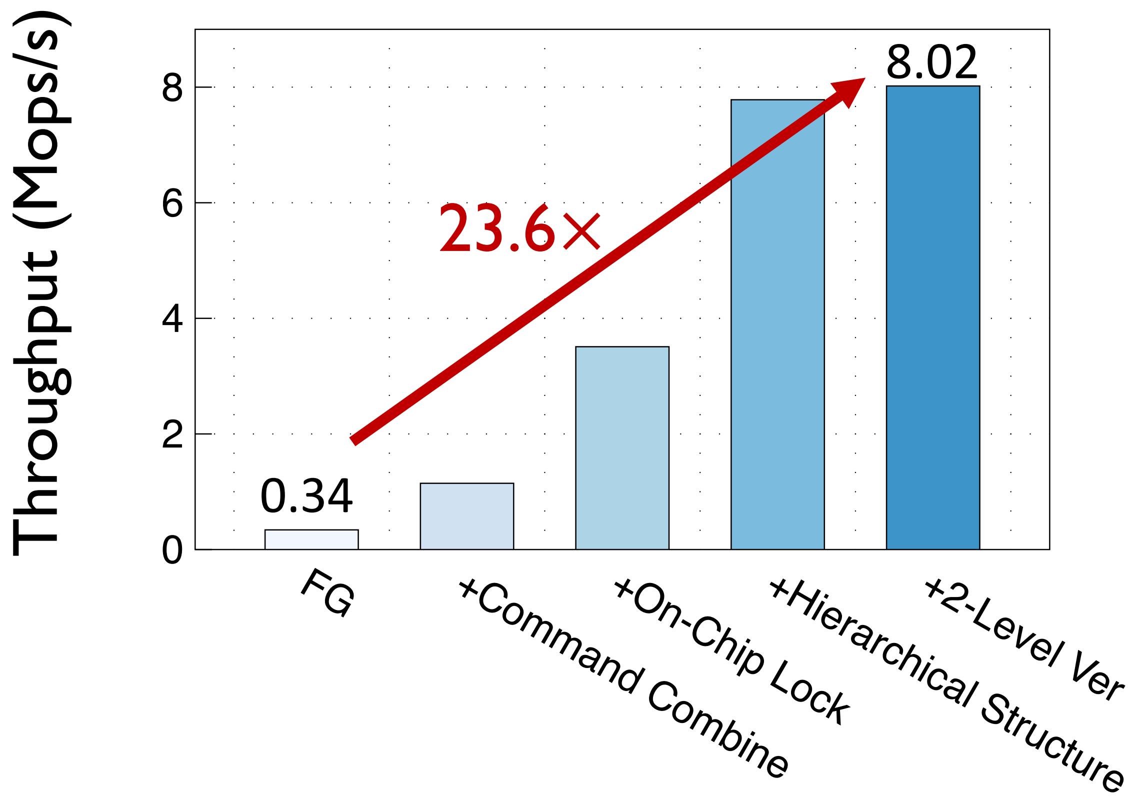
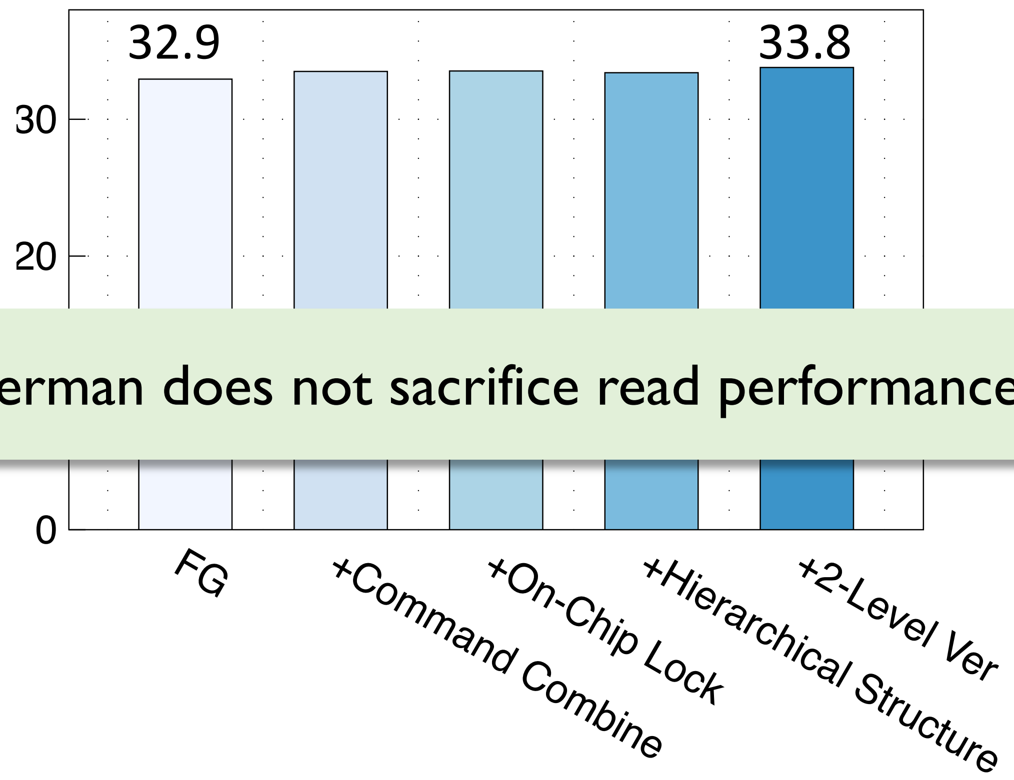
Throughput (176 client threads)

Write-intensive(50% lookup, 50% update/insert)



Read-intensive (95% lookup, 5% update/insert)



Sherman does not sacrifice read performance

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99th Percentile Latency (176 client threads)

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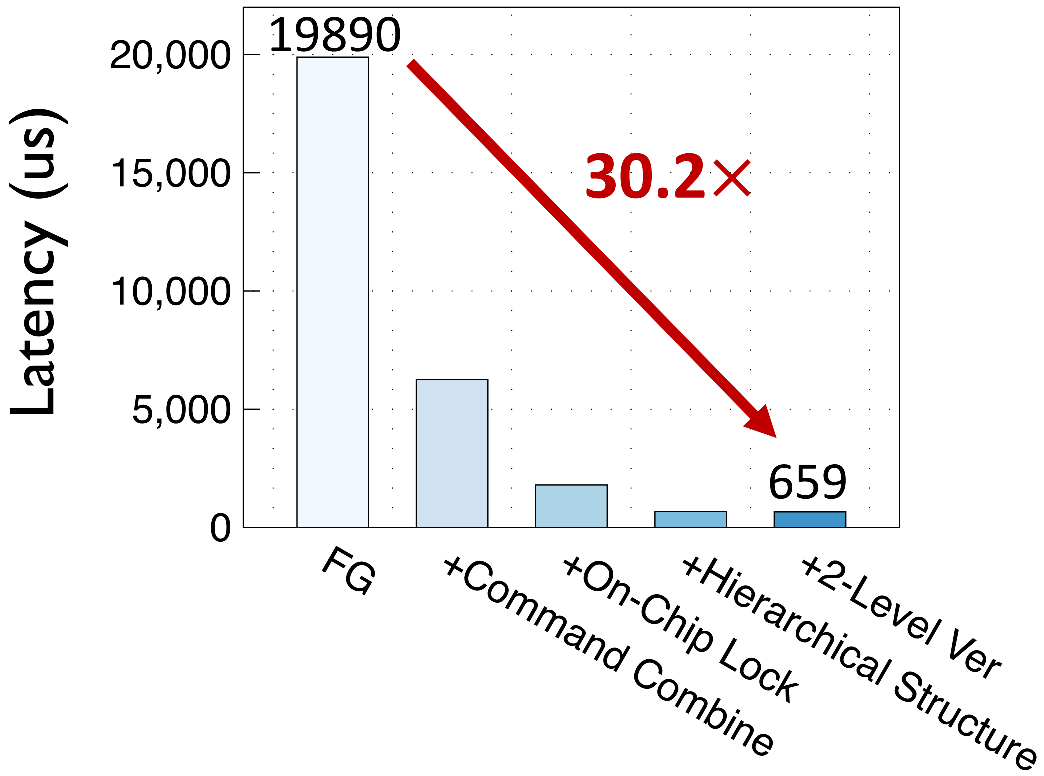

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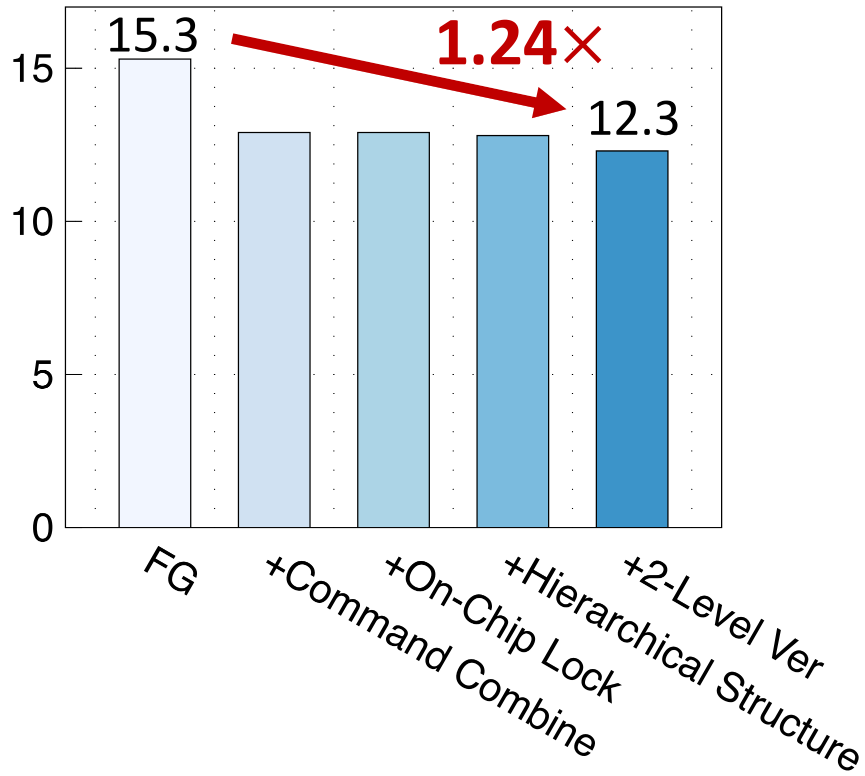

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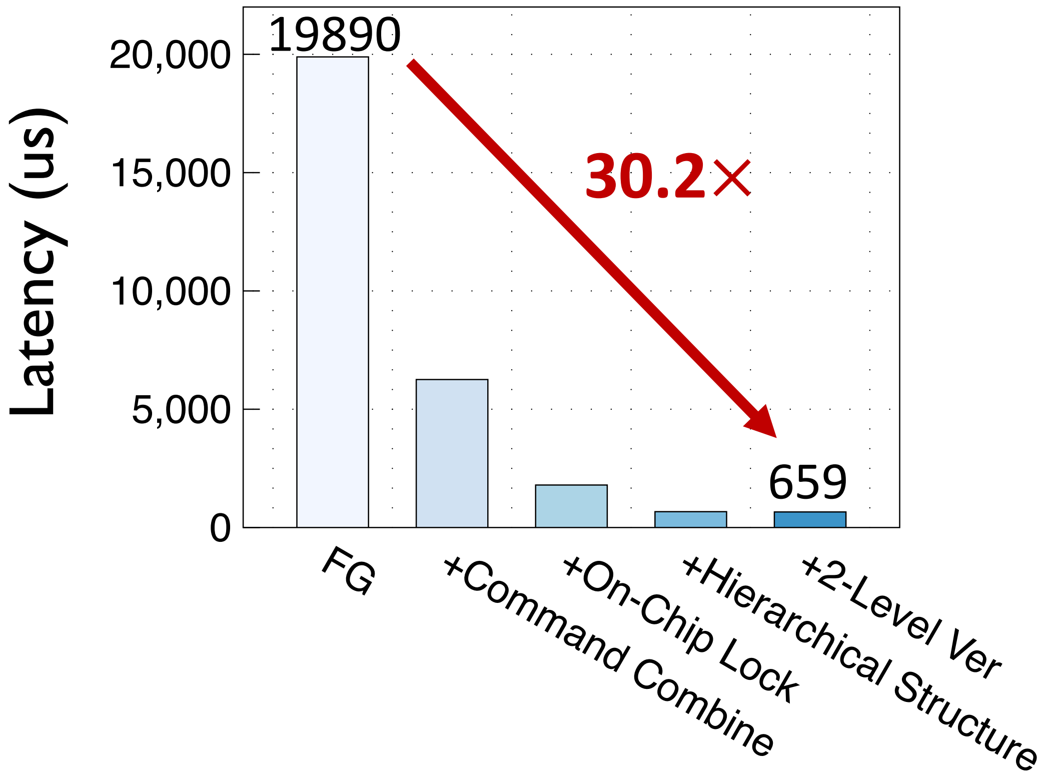

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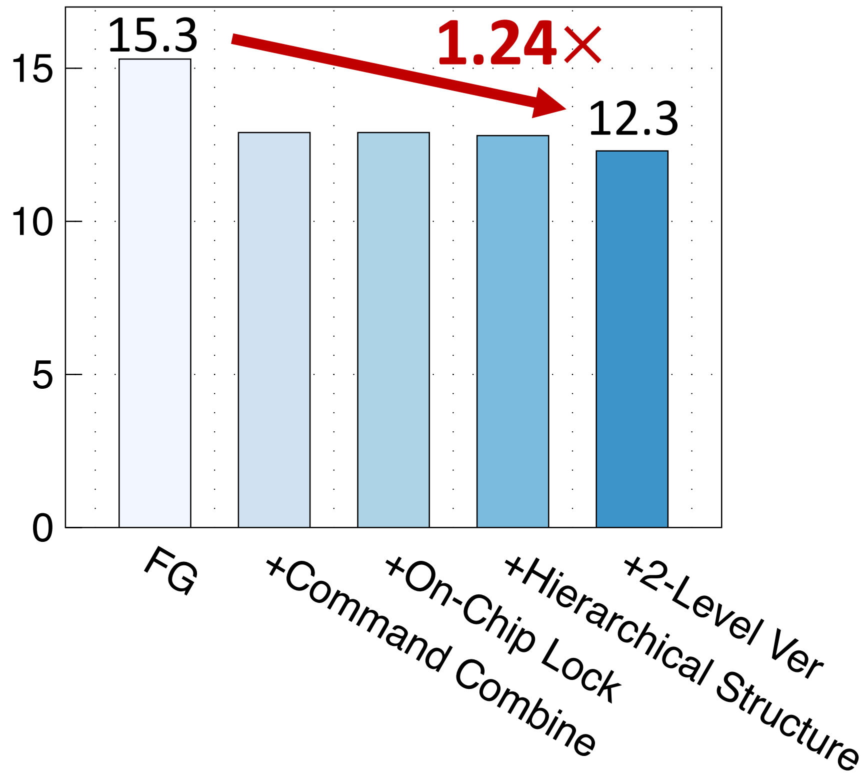

Sherman lowers tail latency by reducing round trips and boosting concurrency efficiency

Outline

- Background & Motivation
- Sherman – A Write-Optimized B+Tree on Disaggregated Memory
- Evaluation
- Summary

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- Goal
  - Building a fast tree index on disaggregated memory with commodity RDMA NICs

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  - Two-level version layout – Mitigating write amplification
- Results
  - Sherman improves throughput and 99th percentile latency by one order of magnitude on typical write-intensive workloads

Thanks & QA

Sherman: A Write-Optimized Distributed B+Tree Index on Disaggregated Memory

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